Amendments to the Claims:

A clean version of the entire set of pending claims, including amendments to the claims, is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) An integrated circuit comprising a set of cells, each cell comprising an electrical device having a device parameter with a parameter value which is a function of random parametric variations, the set of cells comprising:

a first subset of identification cells; and

a second subset of cells for generating an identification code by measuring the parameter values of the identification cells wherein the identification cells have first random parametric variations and the cells of the second subset have second random parametric variations, the first random parametric variations being larger than the second random parametric variations.

2. (Currently Amended) ~~An integrated circuit as claimed in~~ The integrated circuit of claim 1, wherein: the first random parametric variations cause random differences among the parameter values of the identification cells, the random differences each having an absolute value, the absolute values having an average value; and

the second random parametric variations cause an offset in the parameter values of the identification cells, the offset having an absolute value, the average value being larger than the absolute value of the offset.

3. (Currently Amended) ~~An integrated circuit as claimed in~~ The integrated circuit of claim 2, wherein the identification cells each contain only one electrical device.

4. (Currently Amended) ~~An integrated circuit as claimed in~~ The integrated circuit of claim 1, wherein the random parametric variations comprise a random distribution of doping atoms in at least a part of the electrical device.

5. (Currently Amended) ~~An integrated circuit as claimed in~~ The integrated circuit of claim 4, wherein the electrical device comprises a metal oxide semiconductor field effect transistor comprising a source, a drain, a gate, and a channel, which is situated between the source, the drain and the gate, the channel being electrically insulated from the gate by an oxide, the part of the electrical device having the random distribution of doping atoms comprising the channel.

6. (Currently Amended) ~~An integrated circuit as claimed in~~ The integrated circuit of claim 1, wherein the electrical device comprises an ohmic resistor having a resistance value, which is a function of the random parametric variations.

7. (Currently Amended) ~~An integrated circuit as claimed in~~ The integrated circuit of claim 6, wherein the ohmic resistor comprises a silicide material and has a shape, the random parametric variations comprising a random distribution of shapes.

8. (Currently Amended) ~~An integrated circuit as claimed in~~ The integrated circuit of claim 6, wherein the random parametric variations comprise a random distribution of insulating objects in the ohmic resistor.

9. (Currently Amended) ~~An integrated circuit as claimed in~~ The integrated circuit of claim 8, wherein the first subset comprises a random number of identification cells each having ohmic resistors comprising a first part and a second part, which is electrically insulated from the first part by the insulating objects.

10. (Currently Amended) A method for manufacturing an integrated circuit ~~as claimed in claim 1, the integrated circuit~~ comprising a substrate having ~~and a set of~~

~~cells, each cell comprising an electrical device having a device parameter with a parameter value which is a function of random parametric variations, the substrate comprising~~ a first portion and a second portion, the method comprising:

forming a first subset of identification cells in the first portion of the substrate, the identification cells each comprising an electrical device having a device parameter with a parameter value, wherein the identification cells have first random parametric variations;

forming a second subset of cells in the second portion of the substrate, the second subset of cells for generating an identification code by measuring the parameter values of the identification cells, wherein the set of second cells have second random parametric variations; and

~~a step which causes the cells to have the random parametric variations,~~

~~wherein means for~~ increasing the first random parametric variations[[,]] in ~~at least a part of the first portion~~ the first subset of cells with respect to the second random parametric variations in the second ~~portion are applied during at least part of the execution of said step~~ subset of cells to make the first random parametric variations larger than the second random parametric variations.

11. (Currently Amended) ~~A method as claimed in~~ The method of claim 10, wherein ~~during at least a part of the step of applying the means for~~ increasing the first random parametric variations with respect to the second random parametric variations includes covering the second portion ~~is covered by~~with a first mask during at least part of the steps of forming the first and second subsets of cells, ~~which~~ wherein the first mask at least partly prevents an increase of the second random parametric variations ~~in the second portion~~ while permitting an increase in the first random parametric variations.

12. (Currently Amended) ~~A method as claimed in~~ The method of claim 11, ~~wherein the step causing random parametric variations comprises a sub-step causing~~ further comprising introducing at least part of the second random parametric

variations in at least a part of the second portion while the first portion is covered by a second mask ~~which at least partly prevents introducing the random parametric variations in the first portion during the sub-step~~.

13. (Currently Amended) ~~A method as claimed in~~ The method of claim 10, wherein the step ~~causing the random parametric variations~~ of increasing the first random parametric variations with respect to the second random parametric variations comprises implanting doping atoms in the first and second portions such that a variation in the doping atoms in the first subset of cells is increased with respect to a variation in the doping atoms in the second subset of cells.

14. (Currently Amended) ~~A method as claimed in~~ The method of claim 13, wherein ~~the means for~~ increasing the first random parametric variations with respect to the second random parametric variations comprises randomly distributing objects ~~randomly distributed~~ over at least a part of the first portion, the objects at least partly preventing the doping atoms from being implanted.

15. (Currently Amended) ~~A method as claimed in~~ The method of claim 13, wherein at least a part of the doping atoms carry a charge when they are implanted and a deflection unit randomly ~~deflecting~~ deflects the charged doping atoms in the first portion by applying a random deflection signal ~~is used as the means for increasing~~ to increase the first random parametric variations with respect to the second random parametric variations.

16. (New) The integrated circuit of claim 1, wherein the second subset of cells includes a reference cell to produce a reference current.

17. (New) The integrated circuit of claim 16, wherein the second subset of cells includes a load cell for receiving the reference current and a current from a selected one of the identification cells and for outputting a voltage difference

produced by a difference between the reference current and the current from the selected identification cell.

18. (New) The integrated circuit of claim 17, wherein the load cell includes only three transistors:

a first load transistor receiving the reference current,

a second load transistor receiving the current from the selected identification cell, and

a diode-connected transistor providing a bias voltage to the first and second load transistors.

19. (New) The integrated circuit of claim 1, wherein each identification cell includes a first transistor producing a first current and a second transistor producing a second current, the integrated circuit further comprising:

a load cell for receiving the first and second currents from a selected one of the identification cells and for outputting a voltage difference produced by a difference between the first and second currents from the selected identification cell, wherein the load cell includes only three transistors:

a first load transistor receiving the first current from the selected identification cell,

a second load transistor receiving the second current from the selected identification cell, and

a diode-connected transistor providing a bias voltage to the first and second load transistors.